Docket No.: 050432-0592

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Application of	Customer Number: 41552
PAN, JAMES N.	Confirmation Number: 6675
Application No.: 10/614,031	Tech Center Art Unit: 2812
Filed: July 08, 2003	Examiner: Andre C. Stevenson

For: METHOD FOR DETERMINING METAL WORK FUNCTION BY FORMATION OF SCHOTTKY DIODES WITH SHADOW MASK

CERTIFICATE OF FACSIMILE TRANSMISSION
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Brenda Lewis

APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed concurrently herewith.

I. Real Party In Interest

The real party in interest is Advanced Micro Devices, Inc.

II. Related Appeals and Interferences

Appellants are unaware of any related Appeal or Interference.

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III. Status of Claims

Claims 1-18 are pending in this application. Claims 12-18 are allowed, while Claims 4-11 were indicated as allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims. Claims 1-3 have been thrice rejected. Appellants hereby appeal from the Examiner's third rejection of Claims 1-3.

IV. Status of Amendments

An amendment has been filed concurrently with this Appeal Brief to obviate informalities noticed by the Examiner in the third Office Action. Since the amendment addresses only minor informalities, it is assumed that such amendment will be entered.

V. Summary of Claimed Subject Matter

Claim 1 is the only rejected independent claim. The subject matter encompassed by independent Claim 1 is directed to a method of determining the work function of a metal comprising forming a metal-on-silicon (MS) Schottky diode with a metal having a work function to be determined forming contacts of the MS Schottky diode. A capacitance-voltage curve of the MS Schottky diode is measured, and the work function of the metal is determined based on the measured capacitance-voltage curve. (Page 2 of the Written Description , paragraph 9).

The invention defined in independent Claim 1 addresses and solves problems attendant upon screening a large number of potential metal gate materials in an economical and relatively fast manner. (Page 2 of the Written Description, paragraph 8).

In the past, a Schottky diode has been employed to measure an MOS-CV curve to determine the metal work function of the metal materials. These Schottky diodes were formed by employing

traditional lithography, metal deposition and etch processing steps. The Schottky diodes were metal-on-oxide-on-silicon diodes (MOS). The formation of such MOS Schottky diodes by this traditional method is relatively expensive and time-consuming. (Page 2 of the Written Description, paragraph 7).

Embodiments of the present invention show a silicon wafer substrate 10 that has a shadow mask 12 secured onto the top of the substrate 10. The shadow mask 12 may be made of a stainless steel, for example. (Page 4 of the Written Description, paragraph 19). Once the shadow mask 12 is secured in place, a conventional process may be employed to deposit the metal, such as sputter depositing by physical vapor deposition. The metal will be deposited on a silicon substrate. (Page 5 of the Written Description, paragraph 26).

Significantly, dependent Claim 2, the separate patentability of which is argued on appeal, specifies that the step of forming the MS Schottky diode includes depositing the metal on a silicon substrate in accordance with the mask on the silicon substrate. Dependent Claim 3 requires the mask to be a shadow mask. The thin film metal is deposited selectively in the cut out portions of the shadow mask to create the MS Schottky diodes. The use of a shadow mask with repeating patterns with formation of metal-on-silicon (MS) Schottky diodes avoids the traditional lithography, metal deposition and etch processing steps. Instead, the MS Schottky diodes can be built on blanket silicon wafers with a single metal deposition, reducing the time and expense needed to determine the work function of candidate materials for metal gates. (Page 2 of the Written Description, paragraph 9).

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VI. Grounds of Rejection To Be Reviewed By Appeal

Claim 1 was rejected under U.S.C. §103(a) for obviousness predicated upon Rao et al. in view of Yonehara et al.

Claims 2 and 3 were rejected under 35 U.S.C. §103(a) for obviousness predicated upon Rao et al. in view of Yonehara et al. and further in view of McFarland et al.

In the statement of the rejection, the Examiner admits that Rao et al. fails to disclose forming a metal-on-silicon (MS) Schottky diode which is, of course, a significant feature of the claimed invention. The Examiner, nevertheless, concluded that one having ordinary skill in the art would have been motivated to substitute a silicon substrate for the glass substrate of Rao et al. to form a metal-on-silicon (MS) Schottky diode in view of Yonehara et al. The Examiner alleged that Yonehara et al. explicitly taught silicon substrate as a conventional equivalent or alternate to a glass substrate.

VII. Argument

For the convenience of the Honorable Board, the patentability of Claim 1 stands on its own. Appellants also separately argue the patentability of Claims 2 and 3 as a group, predicating the patentability of Claims 2 and 3 upon Claim 2, the separate patentability of which is vigorously advocated.

Independent Claim 1

Rao et al., the primary reference relied upon by the Examiner, addresses the characteristics of Al/p-$Cu_{0.5}Ag_{0.5}$ $InSe_2$ polycrystalline thin film Schottky barrier diodes and reports on the characteristics of such thin film Schottky barrier diodes. The Examiner appears at first to recognize that Rao et al. describes forming a Schottky diode with a metal-on-glass structure. However, the Examiner is not consistent in this recognition. See, Office Action of August 10, page 2, in which the Examiner stated

that Rao et al. shows forming a Schottky diode (metal-on-glass) with a metal having a work function to be determined forming contacts of the metal-on-silicon (MS) Schottky diode, measuring a capacitance-voltage curve of metal-on-silicon (MS) Schottky diode. In fact, the Examiner was correct in his first mention of the Schottky diode as being metal-on-glass. At page 572 of Rao et al., lines 5-8, it states that "all thin film Al/p-$Cu_{0.5}Ag_{0.5}$ In Se_2 Schottky junctions were fabricated in the following matter. Gold films of 500 nm thickness were deposited onto Corning 7059 glass substrates held at 548 K by the thermal evaporation technique onto which a 5000 nm thickness p-$Cu_{0.5}Ag_{0.5}InSe_2$ films were deposited by the flash evaporation technique at 693 K." Hence, the Schottky diode is a metal-on-glass type diode. Yet the Examiner makes the unsupported assertion that Rao et al. discloses that the Schottky diode is formed with the metal having a work function to be determined forming contacts of the metal-on-**silicon** Schottky diode. The Examiner also asserts that Rao et al. discloses measuring a capacitance-voltage curve of the metal-on-**silicon** Schottky diode.

It is apparent that the Examiner has misapprehended the teachings of Rao et al. Since Rao et al. fails to disclose a metal-on-silicon (MS) Schottky diode, the metal having a work function to be determined cannot form contacts with the metal-on-silicon (MS) Schottky diode. Nor can there be a measurement of a capacitance-voltage curve of a metal-on-silicon (MS) Schottky diode in Rao et al. Therefore, these steps must be considered as completely missing in Rao et al. The Examiner's statements to the contrary, and the assertion that Rao et al. shows the method substantially as claimed, must be considered to be in error. In order to supply the missing disclosure or suggestion, the Examiner now turns attention to Yonehara et al. The Examiner asserted that although diamond substrates were exemplified, Yonehara et al. taught conventional substrates which are used to form a Schottky diode, include glass or silicon substrates as equivalents or alternates. However, a closer and thorough examination of Yonehara et al. shows that such reliance is misplaced.

Yonehara et al. describes a method for forming a Schottky diode that utilizes diamond as a semiconductive material (Col. 1, lines 6-7). The Yonehara et al. patent relates to the formation of a diamond layer on a substrate in the formation of a Schottky diode. See, for example, Col. 2, lines 26-29. Further, Yonehara et al. notes that Schottky diodes prepared in the inventive manner are naturally much more uniform in performance than those formed on a random polycrystalline layer. As noted at Col. 4, lines 9-14, Figure 4 shows a structure of Schottky diodes formed on diamond crystals having sufficiently large amounts of crystalline area selectively grown in predetermined positions as explained above. The Schottky diode was prepared by forming the above-explained diamond layer 42 on a P^+ silicon substrate 43, then forming ohmic electrode 44 on the bottom face of the substrate and forming an aluminum electrode 41 on the top face of the diamond layer. Hence, the figure and the written description in Yonehara et al. clearly contemplates the formation of a diamond layer on a silicon substrate, with the aluminum electrode being formed on the diamond layer. This structure is not a metal-on-silicon (MS) Schottky diode, but rather a metal-on-diamond Schottky diode. The Examiner noted that Yonehara et al. explicitly teaches silicon substrate as a conventional equivalent or alternative to a glass substrate, and refers to Col. 4, lines 45-50. However, the different examples of a substrate in this description are employed for the purposes of growing a diamond layer on the top thereof, in conformance with the remainder of the Yonehara et al. patent. The substitutability of a silicon substrate for a glass substrate can legitimately only be extended to the specific structure of Yonehara et al. In other words, Yonehara et al. only describes the substitution of a crystalline silicon substrate or polycrystalline silicon substrate for a glass substrate in a structure in which a diamond layer is formed on such a substrate, with the metal electrode being formed on the diamond layer. It is inappropriate to extrapolate the substitutability of a silicon substrate for a glass substrate in Rao et al. without a clear teaching of the equivalents of such a structure. Yonehara et al. fails to make such a universal

endorsement of the substitutability of a glass substrate for a silicon substrate. It is therefore respectfully submitted that one of ordinary skill in the art would therefore not be motivated by Yonehara et al. to make the substitution of a silicon substrate for the glass substrate over Rao et al. The question of whether the silicon substrate should provide similar results to a glass substrate leads to the inappropriate "obvious to try" standard of determining obviousness. One of ordinary skill in the art has not been provided by Yonehara et al. any motivation that would suggest the substitutability of a silicon substrate of a glass substrate.

At best, since Yonehara et al. teaches forming a metal-on-diamond Schottky diode, even if combined with Rao et al., the two references do not suggest a combination of the present invention. A combination of the references would teach a silicon substrate covered by a diamond coating with an Al/p-$Cu_{0.5}Ag_{0.5}InSe_2$ layer formed to create a polycrystalline thin film Schottky barrier diode. To suggest otherwise would ignore the clear teachings of these references and involve impermissible hindsight. In neither reference is there any teaching of providing metal on silicon.

Dependent Claims 2 and 3

Appellants separately and vigorously advocate the patentability of Claims 2 and 3. Claim 2 depends from Claim 1 which states that the MS Schottky diode is a metal-on-silicon (MS) Schottky diode. Claim 2 further specifies that the step of performing the MS Schottky diode includes depositing the metal on a silicon substrate in accordance with the mask on the silicon substrate. Hence, Claim 2 requires that the metal be deposited on the silicon substrate. Yet, McFarland et al. fails to disclose such a step. As can be seen in Figure 1B, the front metal contact pads 26 are formed on a silicon dioxide layer 28. Similarly, the back ohmic contacts 24 are formed under a backside oxide 25. Hence, McFarland et al. fails to disclose the step of depositing metal on a silicon substrate in accordance with a mask on the silicon substrate. Instead, the metal is deposited on oxide, so that a metal-on-oxide-on-

silicon (MOS) Schottky diode is formed. Claim 3, which requires that the mask is a shadow mask, stands or falls with Claim 2. Even if the references can be combined as proposed by the Examiner, and Appellants do not agree that the requisite fact-based motivation has been established, the claimed invention would not result since none of the references disclose a metal-on-silicon (MS) Schottky diode.

VIII. CONCLUSION

Based on the foregoing, Appellants submit that the Examiner has failed to establish a *prima facie* basis to deny patentability to the inventions defined in independent Claim 1 and in dependent Claims 2 and 3, for lack of the requisite factual basis and want of the requisite realistic motivation. Appellants, therefore, solicit the Honorable Board of Patent Appeals and Interferences, to reverse the Examiner's rejection of the appealed claims under 35 U.S.C. §103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

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CLAIMS APPENDIX

1. A method of determining a work function of a metal, comprising the steps of:

forming a metal-on-silicon (MS) Schottky diode with a metal having a work function to be determined forming contacts of the MS Schottky diode;

measuring a capacitance-voltage cure of the MS Schottky diode; and

determining the work function of the metal based on the measured capacitance-voltage cure.

2. The method of claim 1, wherein the step of forming the MS Schottky diode includes depositing the metal on a silicon substrate in accordance with a mask on the silicon substrate.

3. The method of claim 2, wherein the mask is a shadow mask.

4. The method of claim 2, wherein a first one of the contacts is at least ten times smaller in size than a second one of the contacts.

5. The method of claim 4, wherein the step of measuring a capacitance-voltage curve includes contacting the first and second contacts with respective probes of an LCR meter.

6. The method of claim 5, wherein the first and second contacts are on the same side of the silicon substrate.

7. The method of claim 6, wherein the first contact is at least 100 times smaller in size than the second contact.

8. The method of claim 7, wherein the first contact is at least 800 times smaller in size than the second contact.

9. (original) The method of claim 2, wherein a plurality of the contacts are actual capacitor contacts and another one of the contacts is a front contact.

10. The method of claim 9, wherein the actual capacitor contacts are different sizes from one another.

11. The method of claim 10, wherein each of the actual capacitor contacts have a size that is at least 100 times smaller than the front contact.

12. A method of forming Schottky diodes for determining work function of a metal, comprising the steps of:

positioning a shadow mask having holes on a silicon substrate; and

depositing the metal through holes in the shadow mask into the silicon substrate, the holes including at least a first hole with a first cross-sectional area and a second hole with a second cross-sectional area that is at least 100 times greater than the first cross-sectional area.

13. The method of claim 12, wherein the holes in the shadow mask are in sets of a repeating pattern.

14. The method of claim 13 , wherein each pattern includes actual capacitor holes and a front contact hole, the front contact hole being the second hole, and the actual capacitor holes being the first holes.

15. The method of claim 14, wherein the actual capacitor holes within each one of the patterns are different sizes from one another.

16. The method of claim 15, wherein each of the actual capacitor holes within each pattern is at least 100 times smaller than the front contact holes.

17. The method of claim 16, wherein the front contact hole is approximately .25 in^2.

18. The method of claim 17, wherein a first one of the actual capacitor holes is approximately .02 in in diameter, a second one of the actual capacitor holes is approximately .015in in diameter, and a third one of the actual capacitor holes is approximately .010 in in diameter.